AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1-30 (Cancelled)

31. (Currently Amended) ~~In a multi-threaded processor executing instructions for at least first and second threads, a method of assigning thread priority~~ A method comprising:

determining whether instruction fetch operations for ~~the~~ a first thread will be blocked due to processing of instructions for ~~the~~ a second thread in a multi-threaded processor executing instructions for said first and second threads;

assigning priority to the first thread in said processor based on said determining operation.

32. (Previously Presented) The method of claim 31 further comprising;

setting a threshold counter to perform a counting operation in response to said determining operation.

33. (Previously Presented) The method of claim 32 further comprising:

performing instruction fetch operations for the first thread after said threshold counter completes its counting operation.

34. (Previously Presented) The method of claim 33 further comprising:

moving instructions in an execution pipeline of said processor from the second thread to a temporary storage area.

35 - 38 (Cancelled)

39. (Previously Presented) A multi-threaded processor comprising:

first and second thread queues to store instructions of first and second threads, respectively;

control logic coupled to said first and second thread queues, said control logic to determine whether instruction fetch operations for the first thread will be blocked due to processing of instructions for the second thread.

40. (Previously Presented) The processor of claim 39 wherein said control logic is to assign priority to the first thread in said processor if instruction fetch operations for the first thread will be blocked due to processing of instructions for the second thread.

41. (Previously Presented) The processor of claim 40, further comprising a threshold counter to perform a counting operation, wherein said control logic is to set said threshold counter if it is determined that instruction fetch operations for the first thread will be blocked due to processing of instructions for the second thread.

42. (Previously Presented) The processor of claim 41 wherein said control logic assigns priority to said first thread after said threshold counter completes its counting operation.

43. (Previously Presented) The processor of claim 42 further comprising an execution pipeline and a temporary storage area wherein said control logic is to move instructions in the execution pipeline of said processor from the second thread to the temporary storage area.